Computer Design (CD)

Response to student feedback in 2017/18 course survey

I have taken note of the feedback from students in this course survey, and have the following comments in response:

- Although it is not necessary to have any background knowledge in Verilog before taking this course, some preparatory reading around the subject is always a good idea. During the course, information is given to students explaining how to download a private copy of the Verilog tools from Xilinx for use on a student's own laptop, and two lectures are set aside to cover the Verilog language before it is used in the lab.
- The commments about having more lab sessions and more instructors present was actually responded to during the course last year, i.e. immediately the comment was made, and this resolved the issue. This year we will also run labs with two instructors, hopefully in every lab.

Nigel Topham, September 2018